A C-BAND LOW-NOISE MMIC PHASED ARRAY RECEIVE MODULE

Fazal Ali, Scott Mitchell, Sanjay Moghe, Pang Ho and Allen Podell

PACIFIC MONOLITHICS, INC.
245 Santa Ana Court
Sunnyvale,CA 94086-4512
(408) 732-8000

ABSTRACT

The development of a GaAs monolithic C-Band low noise phased array receive module is presented. This low cost, high yield module contains five monolithic ICs: two gain stages, two active baluns, and a two-bit phase shifter with on-chip active isolator. Also included are logic decoders, level shift circuitry and two MIC LNAs.

The receive module attains 50 dB gain and 2 dB noise figure across the 4 - 6 GHz band and is realized in a small housing (2.2" x 1.1" x 0.6").

INTRODUCTION

Receive modules with low noise figure, high gain, and accurate phase shift capabilities that are small in size and have high yield are vital components for cost effective phased arrays [1]. One recent effort has produced a demonstration of a receive-only phased array [2]. Encouraging results have been obtained for a phased array module operating at S-band [3].

The design, development, and measured results for a C-band phased array receive module are presented here. In order to achieve the required noise figure performance at a minimum cost, a combination of discrete MIC and monolithic ICs is used.

The module is partitioned into discrete circuitry for low noise amplifiers, and monolithic GaAs ICs for gain block and phase shift functions. All the MMIC chips use one-micron gate length ion-implanted GaAs FETs and no via holes. The module contains all of the support circuitry required for system insertion, including logic decode, level shift, and voltage regulation.

SYSTEM ARCHITECTURE

A complete block diagram of the phased array module is shown in Figure 1.

The module is composed of five distinct stages, each stage being assembled on 395 mil carriers and put together in a connectorized housing.

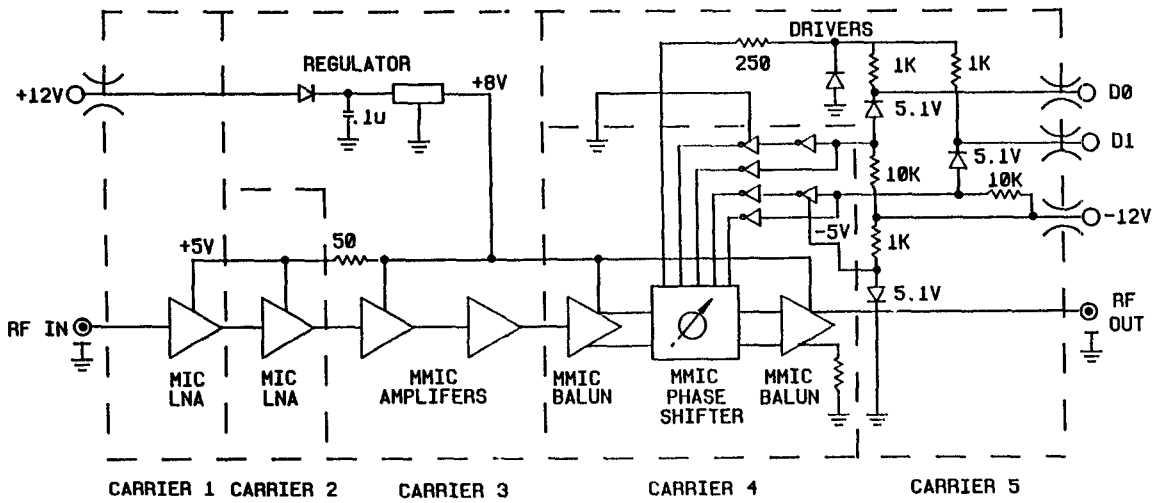

Figure 1. Block Diagram of C-Band Phased Array Receive Module

0149-645X/88/0000-0951$01.00 © 1988 IEEE

MIC LNAs

MMIC LNAs generally have higher noise figures than typical MIC LNAs due to the higher losses associated with monolithic inductors and capacitors. To achieve a very low noise figure (<2 dB) in the 4-6 GHz band, we used discrete low noise FETs (NEC 710) between hybrid Lange couplers for the amplifier. Two LNAs have been built on 395 mil carriers and used in the first two stages of the module.

Gain Blocks

The single-ended monolithic 2-6 GHz amplifier chip (Figure 2) uses a very compact lumped element design and measures only 36 mils square.

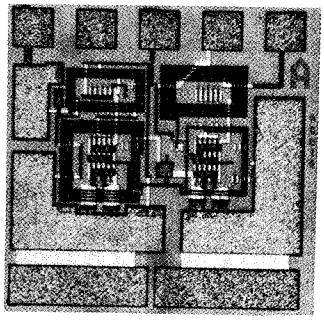

Figure 2. 2-6 GHz Monolithic Single-Ended Amplifier

This two-stage amplifier is designed with two 500 micron FETs and uses a lossy matching technique. With a totem-pole bias scheme, this chip draws 20 mA from a single 8V supply and has 12 dB of gain. The chip has on-chip source bypass capacitors (15 pF each) and an RF choke for DC bias. Two of these chips are cascaded together to achieve 22 dB of gain.

Figure 3 depicts a two-stage monolithic 2-6 GHz active balun. This chip interfaces with the balanced monolithic two-bit phase shifter and the single-ended 2-6 GHz amplifier chip. This active balun operates from a single 8V supply and draws 40 mA. This chip has 7 dB of gain and measures only 48 x 48 mils.

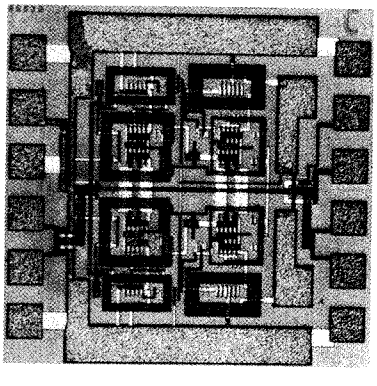

Figure 3. 2-6 GHz Monolithic Active Balun

Phase Shifter

The monolithic two-bit phase shifter chip is implemented as two distinct phase shifter circuits: a 180 degree bit and a 90 degree bit, fully integrated along with an active isolator into a single monolithic IC measuring only 77 x 47 mils.

The 180 degree bit uses four SPDT GaAs FET switches and takes advantage of the push-pull topology resulting in minimum chip size as compared to the conventional switched line realization for 180 degree phase shift. Two control voltages (0 V, -2 V) are required to command the 0 degree and 180 degree phase states. Since GaAs FET switches are used as passive elements, there is no DC power consumption.

The 90 degree bit is composed of two pairs of SPDT switches and filter networks. Low-pass and band-pass lumped element filter networks are designed to obtain the differential 90 degree phase shift. Two control voltages are also required to operate this phase shift network.

A unique component used in this IC design to minimize mismatch error is a monolithic active isolator which presents a good match to both input and output with 1 dB insertion loss and 20 dB reverse isolation over 4-6 GHz band. The active isolator draws about 15 mA from an 8V supply. A photograph of the phase shifter chip is shown in Figure 4.

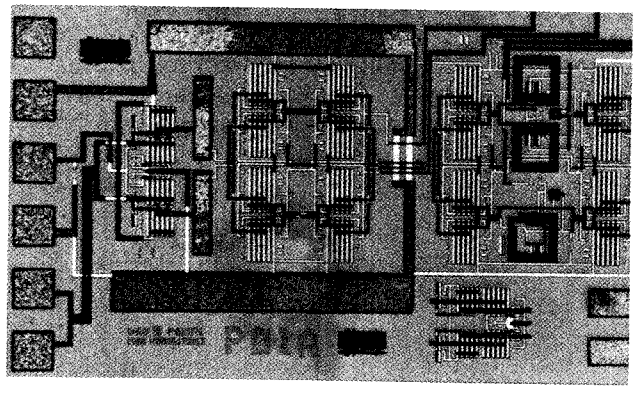

Figure 4. Monolithic 2-Bit Phase Shifter with Active Isolator

Support Circuitry

The two input control lines, D0 and D1 shown in Figure 1, are TTL compatible. Diodes and resistors level shift the signals to a CMOS driver IC, which is used to decode the bits into complementary signals to drive the phase shifter.

RECEIVER SUBSYSTEM RESULTS

The phased array module was tested specifically for the 4-6 GHz band. For the band of interest, the module has a minimum of 50 dB of gain, 2:1 VSWR, 2.2 dB (maximum) noise figure.

The 180^{o} phase shift has a maximum 2^{o} phase error, while the deviation for the 90^{o} and 270^{o} phase states was less than 12^{o} across the band. Amplitude deviation was ± 0.5 dB for all phase states. The performance summary of this module is given in Table 1.

Table 1. Performance Summary

Parameter	Performance
Frequency Range	4.0 - 6.0 GHz
Gain	50 dB minimum
Output Power	5 dBm (8, Sat.)
Noise Figure	2.2 dB maximum
VSWR	1.8:1 (Input) 2:1 (Output)
Gain Deviation (Over all phase states)	< 1 dB
Phase Shift Error:	
0^{o}, 180^{o} State	2^{o}
90^{o}, 270^{o} State	12^{o}
Size	2.2"x1.1"x0.6"

The overall gain response of the complete assembly in all four states (2-bit performance) and the corresponding phase shifts in the 4-6 GHz band are shown in Figures 5 and 6.

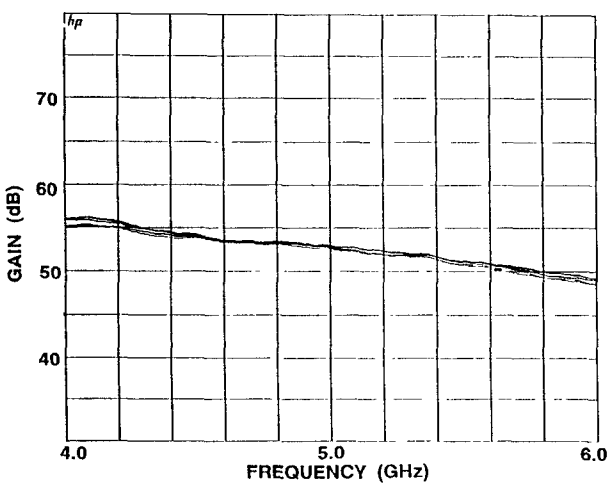

Figure 5. Overall Gain Response of the Complete Module in All Four States

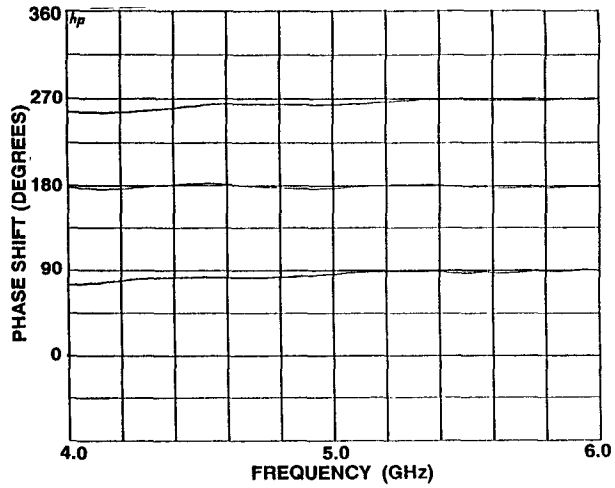

Figure 6. Phase Shift of the Module in All Four States

The overall phase shift (0^{o}, 90^{o}, 180^{o}, 270^{o}) performance of the module over temperature (-40^{o}C to $+65^{o}$C) is depicted in Figure 7.

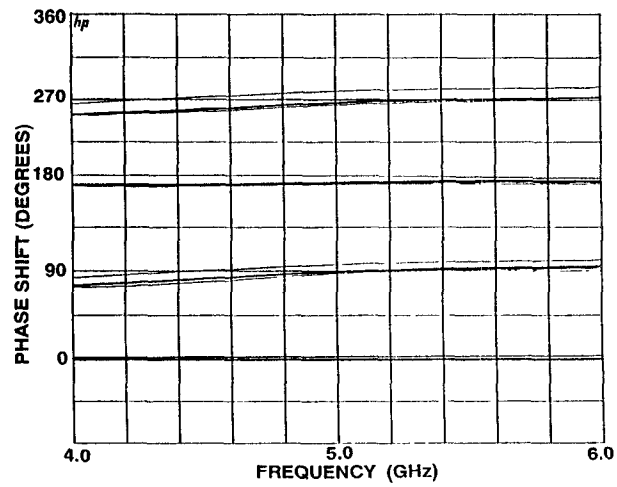

Figure 7. Temperature Performance (-40^{o}C to $+65^{o}$C) of All Four States of the Complete Module

The module was also characterized for a Microwave Landing System (MLS) receiver application. Across 5.0-5.25 GHz, the module has 52 dB of gain and a maximum phase error of 4^{o} and amplitude deviation of $\pm$ .3 dB for the 2-bit performance (0^{o}, 90^{o}, 180^{o}, 270^{o}).

For the phase shifter and gain blocks, MMIC technology and differential lumped element circuit design result in high yield (85%), reproducibility, and good amplitude and phase tracking (less than 1 dB and 5^{o} from unit to unit).

The small chip size for the phase shifter (77 x 47 mils) and gain blocks (36 x 36 mils) allows for compact module realization. A photograph of the subassembly in a housing with SMA connectors is shown in Figure 8. The size of the housing is 2.2" x 1.1" x 0.6".

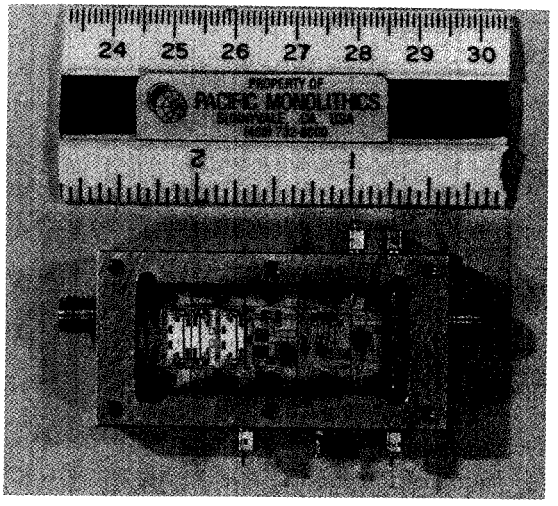

Figure 8. Photograph of the Complete Module in a Housing with SMA Connectors

Future development effort for phased array receive modules will require integration of the low noise amplifier, gain blocks, and multi-bit phase shifter onto a single MMIC chip which will further reduce the size and cost of the module. Initial cost projections indicate $300/module for production quantities. For higher frequency application, similar results can be obtained with 0.5 micron GaAs FET technology.

CONCLUSION

A low cost, compact phased array receive module with 50 dB of gain, 2 dB noise figure, and an accurate two bit phase shifter performance has been fabricated using monolithic and discrete circuits. This prototype effort has successfully demonstrated the feasibility of a phased array receive module in C-band.

ACKNOWLEDGEMENTS

The authors wish to thank Frank Lamb, Bob Genin, Chris Ange, Lucy Ruiz, and Lupe Gonzales for their contributions and help. Special thanks go to Jan Boehm for the preparation of the manuscript.

REFERENCES

1. E. Gregory, "Applicability, Availability, and Affordability of GaAs MMICs to Military Systems," 1986 GaAs IC Symposium, pp. 183-186.

2. G. King and S.J. Flynn, "A Combined MMIC/MIC 8-Channel Receive Only Phased Array Demonstrator Operating in the I/J Band," 1986 IEEE MTT-S Symposium Digest, pp. 535-538.

3. C.R. Green et al., "A 2-Watt GaAs TX/RX Module with Integral Control Circuitry for S-Band Phased Array Radars," 1987 IEEE MTT-S Symposium Digest, pp. 933-936.